

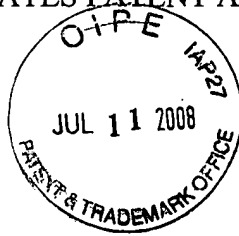
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Prashant Sethi, et al.

Serial No.: 10/806,787

Filed: March 22, 2004

For: A Method And System For Configuration
Of Processor Integrated Devices In Multi-
Processor Systems



§ Group Art Unit: 2181

§
§
§ Examiner: Chun Kuan Lee

§ Atty. Dkt. No.: ITL.1576US
§ (P18870)
§

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

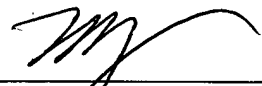
Dear Sir:

Applicants submit the references listed on the attached form PTO 1449, copies of the non-U.S. Patent and Patent Publication references are enclosed.

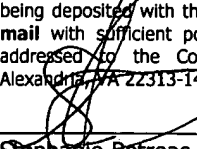
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Respectfully submitted,

Date: 7/8/05



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I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.


Stephanie Petreas